MOŻLIWOŚCI ZASTOSOWANIA TRANZYSTORÓW MOSFET NA BAZIE SiC ORAZ GaN W FAŁOWNIKU KLASY DE

Streszczenie. W początkowej części artykułu przedstawiono podstawowe różnice tranzystorów MOSFET na bazie węglka krzemu (SiC) oraz azotku galu (GaN) w porównaniu do tranzystorów krzemowych (Si). Następnie objąśniono pracę optymalną fałownika klasy DE i zaproponowano jego prosty model, który służy do określenia maksymalnej częstotliwości pracy. Wykorzystując model oraz parametry katalogowe wybranych tranzystorów obliczono, że fałowniki z tranzystorami GaN mogą pracować przy wyższej częstotliwości niż fałowniki z tranzystorami Si i SiC.

Słowa kluczowe: MOSFET, SiC, GaN, fałownik klasy DE

POSSIBLE APPLICATION OF SiC AND GaN MOSFET TRANSISTORS IN CLASS DE INVERTER

Summary: In the initial part of the paper, basic differences between MOSFET transistors based on silicon carbide (SiC) or gallium nitride (GaN) and silicon transistors (Si) are presented. The next part contains explanation of optimal operation mode of Class DE inverter. Simple model of inverter is presented, it is used to estimate maximum operation frequency. It has been evaluated on the basis of this model and parameters from datasheets of selected transistors, that inverter with GaN transistors can operate at higher frequency than inverter with Si and SiC transistors.

Keywords: MOSFET, SiC, GaN, Class DE inverter

1. INTRODUCTION

Subject of the paper is related to investigation of high frequency inverters. Such inverters have been researched for many years in Department of Power Electronics, Electrical Drives and Robotics (Katedra Energoelektroniki, Napędu Elektrycznego i Robotyki - KENER). In this particular case, paper is related to author’s future Ph.D. thesis, which will include analysis of possibilities and limitations in application of MOSFET SiC-based and GaN-based transistors to D, DE and E class inverters in the frequency range of up to 30 MHz.
Relatively new designs of MOSFET transistors are available in the market, based on silicon carbide (SiC) and gallium nitride (GaN). They are characterized by lower drain-to-source on-state resistance $R_{DS(on)}$, smaller parasitic capacitances ($C_{OSS}$, $C_{ISS}$, $C_{RSS}$) and faster switching times ($t_r$, $t_f$) than their counterparts in the same voltage class $V_{DSS}$. In addition, their intrinsic body diode is characterized by very short reverse recovery time $t_{rr}$. This property is most useful in converters with hard switching (e.g. inverters for photovoltaic panels) and drives, since it facilitates reduction in power losses due to transistor switching. Since drain-to-source on-state resistance $R_{DS(on)}$ is also less, converter efficiency is increased and its dimensions are decreased [1].

Class E and DE resonant inverters using SiC-based and GaN-based transistors also show improvement in power parameters. Operation of such inverters with SiC and GaN transistors and switching frequencies of MHz order has been discussed in [2], [3], [4], [5], [6], [7]. In case of GaN-based transistors higher switching frequencies were obtained than in case of SiC-based transistors. High allowable voltage $V_{DSS}$ in SiC-based transistors ($V_{DSS}>1200$ V) means that they are particularly well suited to application in e.g. E class inverter, where peak transistor voltage is about three times as high as supply voltage.

SiC-based and GaN-based transistors require different control parameters than Si-based transistors. The drivers must therefore also be somewhat differently designed.

2. COMPARISON OF Si, SiC and GaN-based MOSFET TRANSISTORS

2.1. SiC-based transistor

We can point out three basic differences between SiC-based and Si-based transistor. The first one is that SiC transistor behaves like voltage-controlled resistor and this results in output characteristic different from that of Si-based transistor (this one behaves like voltage controlled current source). Examples of output characteristics of Si and SiC transistors are shown in Fig.1. In case of Si-based transistors we may observe typical saturation at given gate-source voltage $V_{GS}$ (e.g. $I_d=41$A at $V_{GS}=6$V).
Possible application of SiC...

Second dissimilarity lies in high gate-source voltage. Control voltage recommended by manufacturers is equal to +20V/-5V. Working points at gate-source voltage $V_{GS}=14$V and drain-source voltage $V_{DS}=10$V are marked in curves shown in Fig.1. Transistor currents at these working points are: 120 A for Si-based transistor, and 42 A only for SiC-based transistor. Negative control voltage is recommended for two following reasons:

- So-called parasitic turn-on [10]. This problem occurs in circuits, where two transistor are placed in half-bridge configuration (high and low potential). High voltage rise rate in transistor drain causes a flow of current in gate circuit via capacitance $C_{RSS}$ (Miller capacitance). In particular, if driver impedance is high, this may result in transistor being switched on and also in emergence of cross conduction.

- Low transconductance $g_{fs}$ of SiC-based transistors. This is due to shape of their output characteristic; change in gate-source voltage causes a relatively small change in drain current. Moreover, negative voltage is used in order to accelerate transistor’s switch-off process.

Third difference, which has been mentioned in the introduction, is a fast body diode. Two types of transistors may be distinguished:

- those using intrinsic body diode,
- those including supplementary Schottky diode.

Both diodes are characterized by very small reverse recovery charge $Q_{nr}$ (i.e. short time of recovering blocking properties), but they differ in forward voltage drop $V_{SD}$. Intrinsic body diodes of SiC-based transistors are characterized by high voltage drops; it depends on gate-source voltage $V_{GS}$ (negative $V_{GS}$ voltage will additionally increase $V_{SD}$ voltage). Application of Schottky diode aims to eliminate this problem by decreasing $V_{SD}$ voltage drop and excluding dependence on gate-source voltage. Introduction of Schottky diode leads to increase in transistor’s output capacitance $C_{OSS}$. If converter topology is suitable, then it is...
recommended to adopt method such as the one used in Synchronous Rectification. This consists of switching transistor on in order to redirect diode current to transistor channel. Under such conditions power losses are minimum. Examples of output characteristics for negative (reverse) voltages and currents are shown in Fig.2.

![Fig.2. Output characteristic of SiC transistor for reverse voltages and currents [11]](image)

Rys.2. Charakterystyka wyjściowa tranzystora SiC dla ujemnych napięć i prądów [11]

### 2.2. GaN-based transistors

GaN-based transistors are characterised by much smaller parasitic capacitances than either Si-based or SiC-based transistors. Usually they are manufactured in non-standard packaging in order to minimise lead inductances. In particular, source inductance is most important, since its impact on switching time is most significant. At present (2016) the selection of GaN transistors is not extensive. Recent publications ([2], [3], [4], [6]) show that these transistors may operate at frequency 13.56 MHz without significant problems, when soft switching is applied (ZVS commutation).

They are distinguished by low gate-source voltage (when channel gets saturated) in comparison to other transistor types; this voltage is equal to c. +7 V. Taking into account small values of parasitic capacitances, we obtain total gate-source charge $Q_{GS} < 15$ nC. This is a very small value, since e.g. Si-based transistors DE275 manufactured by IXYS and dedicated to high frequency circuits, are characterised by charge $Q_{GS} = 50$ nC [25]. Output characteristic of GaN-based transistor resembles that of Si-based transistor. We may observe current saturation effect at a given gate-source voltage level (Fig.3).
Fig.3. Output characteristic of NTP8G206N GaN transistor [24]
Rys.3. Charakterystyka wyjściowa tranzystora GaN NTP8G206N [24]

Operation with reverse transistor current is similar as in case of SiC-based transistor with intrinsic body diode (Fig.4b). However, in case of GaN transistor the reverse recovery charge $Q_{rr}$ is ever smaller on account of common base configuration of this transistor [13] (Fig.4a). A low-voltage fast silicon transistor is placed at gate side. This layout is required on account of HEMT (High Electron Mobility Transistor) GaN transistor turned on. In power electronics power transistors should be used as enhancement-mode transistors (“normally closed devices”), since this facilitates design of gate circuits.

Fig.4. a) GaN transistor, common base structure, b) output characteristic for reverse voltages and currents [12]
Rys.4. a) Tranzystor GaN, struktura wspólnej bazy, b) charakterystyka wyjściowa dla ujemnych napięć i prądów [12]
At present (2016) GaN-based transistor manufacturers do not apply external body diodes in order to eliminate problem of output characteristic for reverse voltages and currents. Use of Synchronous Rectification is recommended in application notes.

3. DE CLASS INVERTER

DE class inverter is a power electronics converter which may operate at very high frequencies maintaining very high efficiency at the same time [8], [9]. High efficiency is achieved by means of Zero Voltage Switching (ZVS), which is applied when transistors are switched on and off both. In high-frequency circuits high losses are generated when transistor output capacitances $C_{OSS}$ become short-circuited. ZVS helps to eliminate these losses. DE class inverter scheme is shown in Fig.5. Inverter consists of T1 and T2 transistors together with their drivers DRV, capacitative divider $C_d$, dc voltage source $E$ and $RLC$ circuit. DE class inverters are used mostly for induction heating, supply of plasma chambers, systems for wireless energy transmission, miniature DC/DC converters.

Transistors are switched in turn, with pulse duty factor $D<0.5$, which results in generation of dead time $t_d$ in transistor control (Fig. 6). Inverter may operate at working point which is termed optimum operation. During optimum operation transistor is switched on at zero voltage and zero current (ZVS+ZCS), and switched off at zero voltage and non-zero current (ZVS+NZCS). Under these conditions, switching frequency of the transistors $f$ is slightly higher than resonant frequency of $RLC$ circuit [8]. Appropriate waveforms of current and voltage of low transistor in optimum operation mode are shown in Fig.6.
Further increase of switching frequency (above the level of optimal commutation) results in the fact, that body diodes start to conduct current. This is termed sub-optimal commutation: ZVS occurs during switching on and off. This mode of operation is not analysed in the paper.

If we assume that load current $i$ is sinusoidal, its amplitude is equal to $I_m$, and switching frequency is such that inverter operates in optimal mode (Fig.6), then dead time $t_d = t_{opt}$ required to obtain optimal operation is expressed with formula (1). There $\omega = 2\pi/T$, $T = 1/f$.

$$t_{opt} = \frac{\arccos\left(1 - \frac{2C_{OSS}E\omega}{I_m}\right)}{\omega}$$

(1)

Type of transistors used has a substantial impact on DE class inverter operation. Transistors determine maximum operation frequency and influence output power of the inverter, at specific transistor operating conditions (drain voltage and current). When pulse-duty factor is decreased and optimal mode maintained, operational frequency may be slightly increased [8]. This effect however will be associated with increased recharge time of $C_{OSS}$ capacitance, which leads to reactive power in the circuit and additional losses. Moreover, when frequency is increased, the losses in gate circuit rise and it becomes more and more difficult to achieve a square-wave gate-source voltage. Small total gate charge $Q_G$ makes it possible to decrease these losses and improve shape of voltage waveform.
4. CLASS DE INVERTER MODEL USED IN DETERMINATION OF MAXIMUM OPERATING FREQUENCY

The following assumptions have been adopted for class DE inverter: load current $i$ is sinusoidal, its amplitude is $I_m$, drain-to-source on-state resistance $R_{DS(on)}=0$, output capacitances $C_{OSS}$ are linear and non-zero and transistor switching is instantaneous.

Formula (2) is used to determine inverter’s operating frequency in optimal mode, it is a rearranged form of (1). The dead time $t_d$ has been replaced with a pulse-duty factor $D$, which assumes values ranging from 0 to 0.5.

$$f_{MAX} = \frac{I_m[\cos(2\pi D)+1]}{4\pi EC_{OSS}}$$

Output power $P_{MAX}$ of DE class inverter operating in optimal mode is expressed by formula (3):

$$P_{MAX} = E \cdot I_{DC} = \frac{EI_m}{2\pi} [1 - \cos(2\pi D)]$$

where: $I_{DC}$ is average supply current of the inverter. Relationship (3) has been derived assuming that supply power $P_{DC}=P_{MAX}$ (i.e. inverter is lossless, $R_{DS(on)}=0$).

Power losses in gate circuit $P_{G}$ are described with formula (4). They do not depend on gate resistor values provided that gate capacitances are completely recharged.

$$P_{G} = fQ_{G}U_{GS}$$

where: $Q_{G}$ is gate total charge, $U_{GS}$ is amplitude of gate-source voltage.

5. LISTING OF SELECTED SI, GAN AND SIC BASED TRANSISTORS

Comparison of selected transistors from the viewpoint of their application in DE class inverter is given in this section. For each transistor maximum operating frequency $f_{MAX}$, output power at this frequency $P_{MAX}$ and power losses in gate circuit $P_{G}$ have been determined. Catalogue data has been used for calculations. The following assumptions on transistor operation have been adopted:

- Amplitude $I_m$ of inverter’s output current is equal to rms-value of maximum continuous drain current $I_{D25}$ at 25°C (justification: transistor’s rms drain current $I_D \approx I_m/2 \approx I_{D100}$, $I_{D100} \approx I_{D25}/2$, therefore $I_m \approx I_{D25}$).
- Inverter’s supply voltage $E=0.8V_{DSS}$.
- Pulse-duty factor $D = 0.4$. 
Transistor parameters are set out in Table 1. Real parameters may diverge slightly from those given in Table 1. Calculation of output capacitance $C_{OSS}$ does not take into account non-linearity in the range of low drain-source voltages. Total gate charge has been amended to assumed voltage range (if manufacturer has specified this parameter for some other drain-source voltage). Amplitudes of $U_{GS}$ voltage have been selected keeping in view manufacturer’s recommendations; or, in case of Si-based transistors, a generally accepted standard has been adopted (+12/-5V). Calculations have been run in accordance with formulas (2), (3), (4), results are set out in Table 2.

**Tabela 1. Zestawienie parametrów wybranych tranzystorów**

**Table 1. Comparison of selected transistors’ parameters**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Type</th>
<th>$I_{D25}$ A</th>
<th>$V_{DSS}$ V</th>
<th>$C_{OSS}$ pF</th>
<th>$U_{GS}$ V</th>
<th>$Q_{G}$ nC</th>
</tr>
</thead>
<tbody>
<tr>
<td>APT5010JFLL</td>
<td>Si</td>
<td>41</td>
<td>500</td>
<td>895</td>
<td>17</td>
<td>137</td>
</tr>
<tr>
<td>STP9NK70Z</td>
<td>Si</td>
<td>7.5</td>
<td>700</td>
<td>143</td>
<td>17</td>
<td>61</td>
</tr>
<tr>
<td>VS-FA72SA50LC</td>
<td>Si</td>
<td>72</td>
<td>500</td>
<td>1500</td>
<td>17</td>
<td>310</td>
</tr>
<tr>
<td>C2M0080120D</td>
<td>SiC</td>
<td>36</td>
<td>1200</td>
<td>80</td>
<td>25</td>
<td>63</td>
</tr>
<tr>
<td>CAS120M12BM2</td>
<td>SiC</td>
<td>193</td>
<td>1200</td>
<td>880</td>
<td>25</td>
<td>384</td>
</tr>
<tr>
<td>SCT30N120</td>
<td>SiC</td>
<td>45</td>
<td>1200</td>
<td>130</td>
<td>25</td>
<td>119</td>
</tr>
<tr>
<td>EPC2025</td>
<td>GaN</td>
<td>6.3</td>
<td>300</td>
<td>46</td>
<td>7</td>
<td>3</td>
</tr>
<tr>
<td>GS66516T</td>
<td>GaN</td>
<td>60</td>
<td>650</td>
<td>134</td>
<td>10</td>
<td>18</td>
</tr>
<tr>
<td>NTP8G206N</td>
<td>GaN</td>
<td>17</td>
<td>600</td>
<td>44</td>
<td>10</td>
<td>13</td>
</tr>
</tbody>
</table>

where: $I_{D25}$ is rms-value of maximum continuous drain current at 25°C, $V_{DSS}$ is maximum drain-source voltage.

**Tabela 2. Wyniki obliczeń pracy falownika klasy DE przy pracy optymalnej dla założonego wykorzystania tranzystora**

**Table 2. Calculation results of operation parameters of Class DE inverter in optimal mode for assumed transistor operation**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Type</th>
<th>$f_{MAX}$ MHz</th>
<th>$P_{MAX}$ W</th>
<th>$P_{G}$ W</th>
</tr>
</thead>
<tbody>
<tr>
<td>APT5010JFLL</td>
<td>Si</td>
<td>1.7</td>
<td>4722</td>
<td>4.1</td>
</tr>
<tr>
<td>STP9NK70Z</td>
<td>Si</td>
<td>1.4</td>
<td>1209</td>
<td>1.5</td>
</tr>
<tr>
<td>VS-FA72SA50LC</td>
<td>Si</td>
<td>1.8</td>
<td>8292</td>
<td>9.6</td>
</tr>
<tr>
<td>C2M0080120D</td>
<td>SiC</td>
<td>7.1</td>
<td>9950</td>
<td>11.2</td>
</tr>
<tr>
<td>CAS120M12BM2</td>
<td>SiC</td>
<td>3.5</td>
<td>53345</td>
<td>33.3</td>
</tr>
<tr>
<td>SCT30N120</td>
<td>SiC</td>
<td>5.5</td>
<td>12438</td>
<td>16.3</td>
</tr>
<tr>
<td>EPC2025</td>
<td>GaN</td>
<td>8.7</td>
<td>435</td>
<td>0.2</td>
</tr>
<tr>
<td>GS66516T</td>
<td>GaN</td>
<td>13.1</td>
<td>8983</td>
<td>2.4</td>
</tr>
<tr>
<td>NTP8G206N</td>
<td>GaN</td>
<td>12.2</td>
<td>2349</td>
<td>1.6</td>
</tr>
</tbody>
</table>
5. CONCLUSIONS

- When data contained in Tables 1 and 2 is analysed, we may say that class DE inverters using GaN-based transistors are able to operate at higher frequencies than inverters using Si-based and SiC-based transistors.

- Highest switching frequency may be obtained for inverters using GaN-based transistors. At the same time, gate circuit power losses $P_G$ are very low. This is due to small parasitic capacitances $C_{OSS}$, $C_{ISS}$, $C_{RSS}$ as well as gate-source voltage amplitude $V_{GS}$, which is lower than in other transistors.

- Highest output power may be attained for SiC-based transistors. This results from high maximum drain-source voltage $V_{DSS}$.

- The performed comparison shows that SiC-based transistors may operate at higher frequencies than Si-based transistors. However, taking into account higher control gate-source voltage $U_{GS}$ and large internal gate resistance $R_G$ of SiC-based transistors, the gate voltage inside the transistor may be heavily distorted. Moreover, other parameters may be exceeded, e.g. allowable power losses in gate circuit or in the driver, this will limit the frequency. The model adopted here does not take account of this effect.

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16. Karta katalogowa tranzystora APT5010JFLL
17. Karta katalogowa tranzystora STP9NK70Z
18. Karta katalogowa tranzystora VS-FA72SA50LC
19. Karta katalogowa tranzystora C2M0080120D
20. Karta katalogowa tranzystora CAS120M12BM2
21. Karta katalogowa tranzystora SCT30N120
22. Karta katalogowa tranzystora EPC2025
23. Karta katalogowa tranzystora GS66516T
24. Karta katalogowa tranzystora NTP8G206N
25. Karta katalogowa tranzystora DE275